Please add the following new claims:

28. (new) A wafer dividing method comprising the steps of:

forming grooves in a surface of a wafer, on which surface semiconductor elements are formed, along dicing lines, said grooves being deeper than a thickness of a finished chip;

attaching a holding member on said surface of the wafer on which the semiconductor elements are formed; and

lapping and polishing a bottom surface of the wafer to said thickness of the finished chip, thereby dividing the wafer into chips,

wherein in the step of dividing the wafer into the chips, the lapping and polishing is continued until the thickness of the wafer becomes equal to the thickness of the finished chip, even after the wafer has been divided into the chips by the lapping and polishing.

29. (new) The wafer dividing method according to claim 28 wherein a depth of each groove is greater than the thickness of the finished chip by at least 5 μm.

30. (new) The wafer dividing method according to claim 28 wherein said holding member comprises a substrate coated with an adhesive material.

(new)

31. A method of manufacturing a semiconductor device, comprising the steps of:

forming semiconductor elements in a major surface of a wafer;

forming grooves in said major surface of the wafer along dicing lines, said grooves being deeper than a thickness of a finished chip;

attaching an adhesive sheet on said major surface of the wafer;

lapping and polishing a bottom surface of the wafer to said thickness of the finished chip, thereby dividing the wafer into chips; and

separating each of the divided chips from the adhesive sheet and sealing said each chip in a package,

wherein in the step of dividing the wafer into the chips, the lapping and polishing is continued until the thickness of the wafer becomes equal to the thickness of the finished chip, even after the wafer has been divided into the chips by the lapping and polishing.

(new)

32. The method of manufacturing a semiconductor device, according to claim 31, wherein a depth of each groove is greater than the thickness of the finished chip by at least 5 μm.